## REMARKS

Reconsideration and allowance is respectfully requested. Before entry of this Response, claims 1-23 were pending. In the Office Action, claims 1-23 were rejected. In the present Response, no claims are amended. After entry of the Response, claims 1-23 are pending.

I. Claims 1-7 and 9-23

Claims 1-7, 9-18 and 22-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bongiorno et al. (USP 6,292,045 B1) in view of Lichter et al. (USP 6,970,045 B1) (Office Action, p. 3, lines 1-3). To establish a prima facie case of obviousness, the Examiner must at least demonstrate that the references when combined teach or suggest all of the claimed limitations.

A. Independent claim 1

The combination of Bongiorno and Lichter does not form the basis for a valid rejection of claim 1 under § 103(a) because the references when combined do not teach or suggest either (i) decoupling one clock circuit after decoupling another clock circuit, or (ii) enabling a clock circuit.

(i) Bongiorno does not teach decoupling two clock circuits.

Claim 1 recites decoupling a first clock circuit, coupling a second clock circuit, decoupling the second clock circuit and coupling a third clock circuit. Claim 1 recites "(b) decoupling the first clock circuit . . . (c) coupling a second clock circuit . . . (d) enabling a third clock circuit . . . (e) decoupling the second clock circuit . . . and (f) coupling the third clock circuit . . .". In the Office Action, the Examiner repeats verbatim his argument presented in the Office action dated September 28, 2006, except for citing additional passages of Bongiorno that were not addressed in Applicant's previous response. The additional passages are

lines 8-12 of column 5 and the Abstract of Bongiorno. The entirety of the passages of Bongiorno now cited by the Examiner is reproduced below:



signals has been received. Finally, the controller **40** provides the selected clock signal to a counter or timer **70**. It should be noted that the inventive circuit **100** maybe modified so as to provide the selected clock signal to any device that requires a clock signal in order to operate. Such a device may be a microprocessor **80** as shown in FIG. **1**B, a digital signal processor, an application-specific integrated circuit, a reduced instruction set computer, or a microcontroller.

Referring again to FIG. **1**A, the timer **70** may be a component of a microprocessor-based chip or an integrated circuit that also contains a microprocessor. If so, the timer **70** is preferably a watchdog timer that generates a signal to reset the microprocessor and disable the integrated circuit when the integrated circuit experiences a control failure or a lockup. In this embodiment, the programmed code received by the controller **40** designates the clock source **10** as a first choice for providing the clock signal to the timer **70**. Thus, clock sources **20** and **30** are essentially safety means from which the timer **70** secures a clock signal in order to operate when the clock source **10** becomes malfunctioned and no longer generates any clock signal.

Regarding the controller **40**, it may include a detector **50** and a clock signal selector **60**, both of which receive the clock signals from the clock sources **10**, **20** and **30**. The detector **50** generates a clock source availability signal that indicates whether the clock signals of the clock sources **10**, **20** and **30** have been received. Thereby, the clock source availability signal is provided to the clock signal selector **60** of the controller **40**. In addition, the clock signal selector **60** is programmable to choose one of the clock signals designated by the programmed code. Based on the clock source availability signal and the programmed code, the clock signal selector **60** selects the designated clock signal when the designated clock signal has been received. Otherwise, the clock signal selector **60** automatically selects one of the undesignated clock signals when the designated clock signal has not been received and when at least one of the undesignated clock signals has been received.

With respect to the detector **40**, it may include a delay circuit **54** and three logic gates **55**, **56** and **57** as illustrated by FIG. **2**A. The delay circuit **54** receive first, second and third clock signals from the clock sources **10**, **20** and **30** of FIG. **1**, respectively. Similarly, the logic gates **55**, **56** and **57** receive the first, second and third clock signals, respectively. After the delay circuit **54** receives the first, second and third clock signals (e.g., see FIG. **2**B), it outputs three time-delayed clock signals (e.g., see FIG. **2**C) to the logic gates **55**, **56** and **57**. Then, the logic gates **55**, **56** and **57** respectively output first, second and third signals that indicate whether the first, second and third clock signals have been received, respectively. Thereby, the first, second and third signals are inputted into the clock signal selector **60** of FIG. **1**. Alternatively, the first, second and third signals may be provided to respective low pass filters (not shown) that are respectively coupled between the logic gates **55**, **56** and **57** and the clock signal selector **60** so as to output respective DC signals of the first, second and third signals as input signals to the clock signal selector **60**. In the preferred embodiment, the logic gates **55**, **56** and **57** may be either an exclusive OR gate or an exclusive NOR gate.

With respect to the clock signal selector **60**, it may include an instruction latch or instruction register **62** for storing the programmed code within the clock signal selector **60**, a decoder **64** for translating the content of the instruction register **62** to a meaningful operation or instruction, and a switching means **66** for receiving the clock signals from the clock sources **10**, **20** and **30**. Based on the received clock



source availability signal and the received programmed code, the clock signal selector **60** generates and thereby provides a control signal to the switching means **66**. In response, the switching means outputs one of the clock signals selected by the clock signal selector to the timer **70**. In a preferred embodiment, the switching means is a multiplexer.

Referring to FIG. **1**B, the microprocessor **80** may also be coupled to all three clock sources **10**, **20** and **30** via the inventive circuit **100**. For this embodiment, the above discussion regarding how the inventive circuit **100** of FIG. **1**A operates applies here. It should also be noted that if only one

(57) **ABSTRACT**

A circuit for detecting and selecting one of clock signals of at least two clock sources, is provided. The circuit is coupled to the available clock sources so as to receive their clock signals. The circuit is programmable to choose one of the clock signals designated by a programmed code. Then, the circuit [1] selects the designated clock signal when it has been received and [2] automatically selects the undesignated clock signal when the designated clock signal has not been received and when the undesignated clock signal has been received. Thereafter, the circuit provides the selected clock signal to any device that requires a clock signal in order to operate.

(Bongiorno, col. 4, line 1 – col. 5, line 12; Abstract). Again, Applicants counter that the cited passages of Bongiorno do not teach decoupling a first clock circuit, coupling a second clock circuit, decoupling the second clock circuit, and coupling a third clock circuit. Bongiorno does not teach decoupling one clock circuit after decoupling another clock circuit. Instead of more particularly pointing out where Bongiorno teaches decoupling one and then another clock circuit, the Examiner

expands the cited passages of Bongiorno that allegedly teach the limitations of claim 1. But nowhere in the cited passages above does Bongiorno teach coupling a third clock circuit after decoupling a second clock circuit after coupling the second clock circuit after decoupling a first clock circuit. Bongiorno teaches only switching to one clock from another clock.

The newly cited Abstract of Bongiorno states that the circuit of Bongiorno selects one clock signal. The Abstract states, "A circuit for detecting and selecting one of clock signals . . ." (emphasis added). The cited passage also states that the circuit of Bongiorno selects one clock signal. Lines 35-38 of column 4 of Bongiorno state, "the clock signal selector 60 automatically selects one of the undesignated clock signals when the designated clock signal has not been received and when at least one of the undesignated clock signals has been received." Elsewhere, Bongiorno also teaches that one of the undesignated clock signals is selected. Bongiorno explains, "the controller 40 selects the designated clock signal when the controller 40 has received the designated clock signal. Otherwise, controller 40 automatically selects one of the undesignated clock signals when the designated clock signal has not been received and when at least one of the undesignated clock signals has been received" (Bongiorno, col. 3, line 62 – col. 4, line 1) (emphasis added).

Even when there are more than three alternative clock sources, Bongiorno selects only one undesignated clock signal when the designated clock signal is not available. Bongiorno does not teach decoupling the selected clock signal after decoupling an unavailable clock signal. Bongiorno explains:

> "Table 2 illustrates the priority scheme with respect to four clock sources 1-4. For example, if the instruction register of the clock signal selector receives a programmed code "01011", the decoder of the clock signal would decode this programmed code so that the clock signal selector would select the clock signal from the clock source 2 when the clock source 2 is available regardless of whether the clock sources 1, 3 and 4 are available or not. If the clock source 2 is not available, the clock signal selector would select the clock source 4 when the clock source 4 is available regardless of whether

> the clock sources 1 and 3 are available or not. If the clock sources 2 and 4 are not available, the clock signal selector would select the clock source 3 when the clock source 3 is available regardless of whether the clock source 1 is available or not. Only when all three clock sources 2-4 are not available, the clock signal selector would select the clock source 1." (Bongiorno, col. 7, lines 25-34)

Therefore, only one alternative clock is selected depending on the programmed code and the availability of the alternative clocks. Thus, Bongiorno does not teach (i) deselecting a first clock source (10), (ii) then selecting a second clock source (20), (iii) then deselecting the second clock source (20), and (iv) then selecting a third clock source (30), as the Examiner states.

Lichter also does not teach decoupling one clock circuit after decoupling another clock circuit.

(ii) No proper prior art teaches enabling a clock circuit.

The Examiner admits that "Bongiorno fails to disclose the method comprising the step: (d) enabling a third clock circuit" (Office Action, p. 4, lines 1-2).

The disclosure of the Lichter Patent 6,970,045 may not properly be cited as prior art against the present application 10/764,391 because Lichter was filed on February 19, 2004, which was after the present application 10/764,391 was filed on January 23, 2004. Although the Lichter Patent 6,970,045 does claim priority to a provisional application 60/482,557 filed on June 25, 2003, before the present application, the Examiner has not shown that the disclosure of the provisional application teaches enabling a third clock circuit. In fact, the sparse disclosure of provisional application 60/482,557 does not teach enabling a clock circuit.

The combination of Bongiorno and Lichter does not form the basis for a valid rejection of claim 1 under § 103(a) because Bongiorno and the Lichter provisional application do not teach either (i) coupling and decoupling more than two clock circuits, or (ii) enabling a clock circuit.

Reconsideration of the § 103(a) rejection and allowance of claim 1 are requested.

B. Dependent claims 2-7, 9-10 and 22-23

Claims 2-7, 9-10 and 22-23 depend from claim 1 and are allowable for at least the same reasons for which claim 1 is allowable. Reconsideration of the § 103(a) rejection and allowance of claims 2-7, 9-10 and 22-23 are requested.

C. Independent claim 11

The combination of Bongiorno and Lichter does not form the basis for a valid rejection of claim 11 under § 103(a) because no proper cited prior art teaches turning on a clock circuit upon detecting that another clock circuit has failed.

The Examiner admits that Bongiorno fails to disclose a clock controller adapted to turn on a third clock circuit. (Office Action, p. 8, lines 1-2)

The disclosure of the Lichter Patent 6,970,045 may not properly be cited as prior art against the present application because Lichter was filed after the present application was filed. Although the Lichter Patent 6,970,045 does claim priority to a provisional application 60/482,557 filed before the present application, the Examiner has not shown that the disclosure of the provisional application teaches turning on a clock circuit upon detecting that another clock circuit has failed. In fact, the sparse disclosure of provisional application 60/482,557 does not teach turning on a clock circuit upon detecting that another clock circuit has failed.

Because neither Bongiorno nor the Lichter provisional application teaches a clock controller adapted to turn on a replacement clock circuit upon detecting that the primary clock has failed, reconsideration of the § 103(a) rejection and allowance of claim 11 are requested.

D. Dependent claims 12-18

Claims 12-18 depend directly or indirectly from claim 11 and are allowable

for at least the same reasons for which claim 11 is allowable. Reconsideration of the § 103(a) rejection and allowance of claims 12-18 are requested.

E. Independent claim 19

The combination of Bongiorno and Lichter does not form the basis for a valid rejection of claim 19 under § 103(a) because no proper cited prior art teaches the recited means that turns on a clock circuit upon detecting that a clock signal is inadequate.

The Examiner admits that Bongiorno fails to disclose a clock controller adapted to turn on a third clock circuit upon detecting that a first clock signal is inadequate. (Office Action, p. 11, lines 3-4)

The disclosure of the Lichter Patent 6,970,045 may not properly be cited as prior art against the present application because Lichter was filed after the present application was filed. Although the Lichter Patent 6,970,045 does claim priority to a provisional application 60/482,557 filed before the present application, the Examiner has not shown that the disclosure of the provisional application teaches the recited means that turns on a clock circuit upon detecting that a clock signal is inadequate. In fact, the sparse disclosure of provisional application 60/482,557 does not teach turning on a clock circuit upon detecting that a clock signal is inadequate.

Because neither Bongiorno nor the Lichter provisional application teaches the recited means that turns on a clock circuit upon detecting that a clock signal is inadequate, reconsideration of the § 103(a) rejection and allowance of claim 19 are requested.

F. Dependent claims 20-21

Claims 20-21 depend from claim 19 and are allowable for at least the same reasons for which claim 19 is allowable. Reconsideration of the § 103(a) rejection and allowance of claims 20-21 are requested.

II. Claim 8

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bongiorno in view of Lichter in further view of Chen et al. (US Pat. Pub. 2002/0091785) (Office Action, p. 12 lines 3-5).

The 3-way combination of Bongiorno, Lichter and Chen does not form the basis for a valid rejection of claim 8 under § 103(a) because none of Bongiorno, the Lichter provisional application or Chen teaches (i) all of the limitations of base claim 1, or (ii) the additional limitations of claim 8.

Claim 8 includes the following limitations of base claim 1, "enabling a third clock circuit". None of Bongiorno, Lichter or Chen teaches enabling a clock circuit. For the reasons stated above with regard to claim 1, neither Bongiorno nor the Lichter provisional application teaches enabling a clock circuit. The Lichter Patent 6,970,045 is not proper prior art. Chen also does not teach enabling or turning on a clock circuit.

In addition to the limitations of base claim 1, claim 8 recites "disabling a failure detection circuit that performed the detecting in (a)". The Examiner states that "Chen teaches a clock detection circuit wherein the clock detector can be disabled (column 4, lines 38-51)" (Office Action, p. 12, lines 18-19) (emphasis added). But neither claim 1 nor claim 8 recites "a clock detection circuit". The Examiner has not established a *prima facie* case of obviousness because the Examiner has not stated that Chen teaches "a failure detection circuit". The passage of Chen cited by the Examiner teaches a "fast clock detect logic 122" that detects a faster clock as opposed to a failed clock. The cited passage teaches the detection of a faster clock: "The circuit 100 may provide automatic detection and configuration of FIFOs to device blocks to a faster clock." (Chen, col. 4, lines 45-47). Thus, Chen does not teach disabling a failure detection circuit.

Reconsideration of the § 103(a) rejection and allowance of claim 8 are requested.

III. Conclusion

In view of the foregoing remarks, Applicants respectfully submit that the entire application (claims 1-23 are pending) is in condition for allowance. Applicants respectfully request that a timely Notice of Allowance be issued in this case. If the Examiner would like to discuss any aspect of this application, the Examiner is requested to contact the undersigned at (925) 550-5067.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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